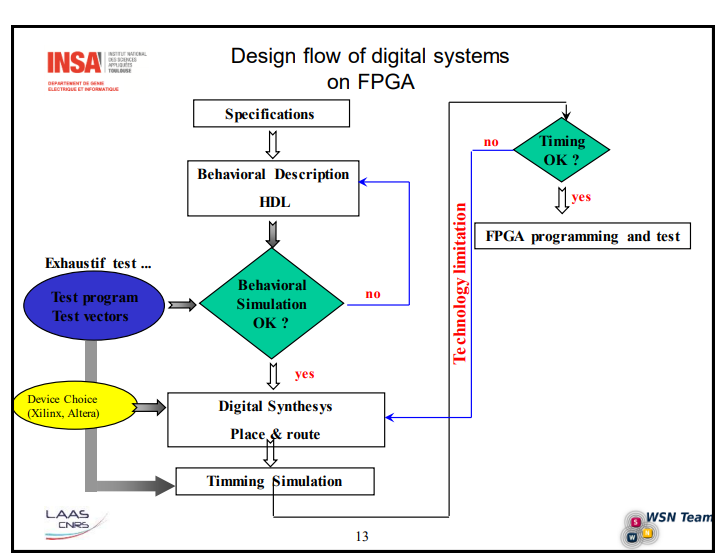
Digital FPGA and ASIC flows summary

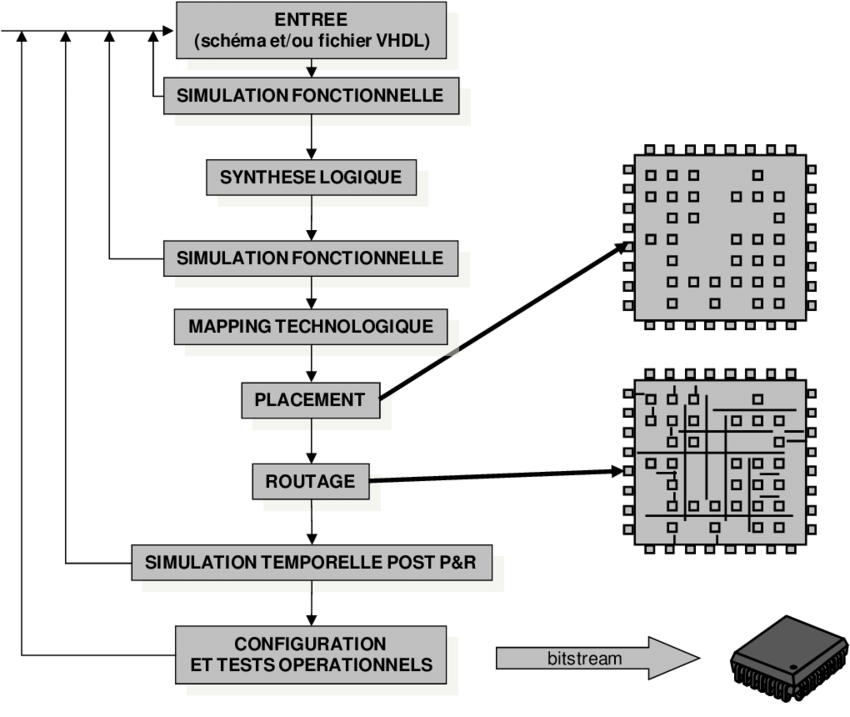
# FPGA:

Software used Xillinx vivado functions:

* Edit RTL descriptions and test benches in VHDL or Verilog
* Simulation with RTL descriptions and test benches files (behavior, post-synthesis, post-par)
* Synthesis
* Implementation (placement and routing)
* Generate bitstream to load on FPGA.

This software also generates reports and summaries to look at TNS (total negative slack), critical path, resources used (LUT…etc) and help to improve RTL description to enhance resources use. Below are two charts representing the digital FPGA flow. Courses and documents about how to use VHDL efficiently to improve critical paths and others are present in the folder “cours utiles”.





These charts are two way representing the FPGA flow.

# ASIC

Contrary to the FPGA flow, we can’t do all the different states with only one software (Xillinx Vivado for example). The ASIC require one software to do simulations, one for synthesis and one for placement and routing. The one I used to learn are the following:

* Simulation(behavioral, post-synthesis, post-placement&routing): Modelsim from SIEMENS (formerly MENTORGRAPHICS)
* Synthesis: Design Vision from Synopsys
* Placement and routing: EDI from Cadence

I used all this tools in a Linux OS and this tools are mostly use with TCL (Tool Command Language) scripts and not a lot with the graphical interface. In the next pages I will give an example of scipts and describe them quickly for each software. But before that you can find two charts representing the ASIC flow.

